



Sheet 1 of 1

Form 1449*	Atty. Docket No.: 1365.048US1	Serial No. 09/898,752
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Sunil Talwar et al.	Group: 2124
	Filing Date: July 3, 2001	

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## U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
<del>JS</del>	3,634,658	01/11/1972	Brown, R.R.	235	92	03/19/70
<del>JS</del>	3,757,098	09/04/1973	Wright, C.M.	235	175	05/12/72
<del>JS</del>	4,607,176	08/19/1986	Burrows, J.L., et al.	307	449	08/22/84
<del>JS</del>	5,095,457	03/10/1992	Jeong, H.	364	758	02/01/90
<del>JS</del>	5,175,862	12/29/1992	Phelps, A.E., et al.	395	800	06/11/90
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**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
<del>JS</del>	0741354	11/06/1996	European	G06F	7/50	
<del>JS</del>	2016181	09/19/1979	United Kingdom	G06F	7/39	
<del>JS</del>	2062310	05/20/1981	United Kingdom	G06F	7/52	
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<del>JS</del>	Booth, A.D., "A Signed Binary Multiplication Technique", <u>Oxford University Press</u> , Reprinted from Q.J. Mech. Appl. Math. 4:236-240, pp. 100-104, (1951)
<del>JS</del>	Dadda, L., "On Parallel Digital Multipliers", <u>Associazione Elettrotecnica ed Elettronica Italiana</u> , Reprinted from Alta Freq. 45:574-580, pp. 126-132, (1976)
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<del>JS</del>	Fleisher, H., "Combinatorial Techniques for Performing Arithmetic and Logical Operations", <u>IBM Research Center</u> , RC-289, Research Report, pp. 1-20, (July 18, 1960)
<del>JS</del>	Foster, C.C., et al., "Counting Responders in an Associative Memory", <u>The Institute of Electrical and Electronics Engineers, Inc.</u> , Reprinted, with permission, from IEEE Trans. Comput. C-20:1580-1583, pp. 86-89, (1971)
<del>JS</del>	Ho, I.T., et al., "Multiple Addition by Residue Threshold Functions and Their Representation By Array Logic", <u>The Institute of Electrical and Electronics Engineers, Inc.</u> , Trans. Comput. C-22: 762-767, pp. 80-85, (1973)
<del>JS</del>	Jones, R.F., et al., "Parallel Counter Implementation", <u>Conf. Rec. 26th Asilomar Conf. Signals, Systems &amp; Computers</u> , Vol. 1, ISBN 0-8186-3160-0, pp. 381-385, (1992)

Examiner <u>D.H. Malzahn</u>	Date Considered <u>5/19/04</u>
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## OTHER DOCUMENTS

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Initial

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	Swartzlander, Jr., E.E., "Parallel Counters", <u>Institute of Electrical and Electronic Engineers, Inc., Reprinted, with permission from IEEE Trans. Comput., C-22:1021-1024, pp. 90-93, (1973)</u>
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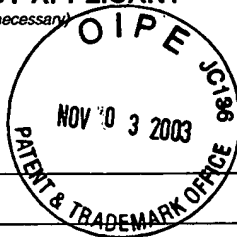
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Application Number	09/898752
Filing Date	July 3, 2001
First Named Inventor	Talwar, Sunil
Group Art Unit	2121
Examiner Name	Unknown

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	WO-99/22292	05/06/1999	Verbauwhede, Ingrid			

## OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
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		DEBNATH, D. , "Minimization of AND-OR-EXOR Three-Level Networks with AND Gate Sharing", IEICE Trans. Inf. & Syst., E80-D, 10, (1997),pp. 1001-1008	
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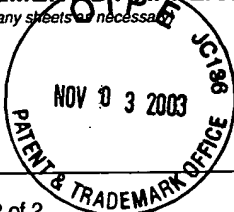
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**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
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<i>[Signature]</i>		ZURAS, D , et al., "Balanced delay trees and combinatorial division in VLSI", IEEE Journal of Solid State Circuits, SC-21, IEEE Inc, New York, Vol. SC-21, no. 5, (1986), 814-819	
<i>[Signature]</i>		PCT International Search Report for corresponding application no. PCT/GB02/01343, international filing date 21 March 2002, mailing date 27 December 2002, four pages	

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